LISTING OF THE CLAIMS

1. (Original) A clock control device which controls the number of pulses of an operation clock to a microprocessor at least based on whether or not there is a bus busy signal indicating a bus busy state from said microprocessor, comprising:

clock control means which supplies the microprocessor with a system clock while the bus busy signal is existing and which supplies the microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing, respectively as an operation clock.

2. (Original) The clock control device according to claim 1, wherein in the case where an interrupt signal based on any of interrupt factors is supplied to the microprocessor, pulse number control data that is set in advance corresponding to the interrupt factor is transferred to the clock control means by a program through the bus from the microprocessor to be set as microprocessor-clock-pulse-number control data, and the number of microprocessor operation clock pulses is controlled.

3. (Original) The clock control device according to claim 1, wherein in the case where an interrupt signal based on any of interrupt factors is supplied to the clock control means, pulse number control data that is set in advance corresponding to said interrupt factor is set as microprocessor-clock-pulse-number control data, and the number of microprocessor operation clock pulses is controlled.

4. (Original) A microprocessor comprising a clock control device, wherein the clock control device includes, clock control means which supplies a microprocessor with a system clock while a bus busy signal is existing and which supplies said microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing, respectively as an operation clock.

5. (Original) An electronic apparatus comprising as control processing means a microprocessor having a clock control device, wherein said clock control device includes clock control means which supplies a microprocessor with a system clock while a bus busy signal is existing and which supplies said microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing, respectively as an operation clock.

6. (Original) A clock control method in which the number of pulses of an operation clock to a microprocessor is controlled at a source supplying the operation clock at least based on whether or not there is a bus busy signal indicating a bus busy state from said microprocessor, comprising the steps of:

supplying the microprocessor with an operation clock of the same pulse number as a system clock while the bus busy signal is existing; and

supplying the microprocessor with a clock having random gap of a reduced number of pulses of the system clock while said bus busy signal is not existing.

7. (Original) The clock control method according to claim 6, further comprising the step of:

prior to an execution of said step of supplying the clock having random gap, setting pulse number control data that is set in advance corresponding to each interrupt factor based on an interrupt signal in accordance with each interrupt factor to the microprocessor as microprocessor-clock-pulse-number control data by transferring to a source supplying the operation clock through the bus from the microprocessor by a program.

8. (Original) The clock control method according to claim 6, further comprising the step of:

prior to an execution of said step of supplying the clock having random gap, setting pulse number control data that is set in advance corresponding to an interrupt factor based on an interrupt signal in accordance with any of interrupt factors to a source supplying an operation clock as microprocessor-clock-pulse-number control data.

9. (Original) A clock control program which controls the number of pulses of an operation clock to a microprocessor at a source supplying the operation clock in accordance with a pulse number control data based on an interrupt signal supplied to the microprocessor from the outside, executing the processing that includes:

an interrupt factor distinction step of distinguishing an interrupt factor each time when the interrupt signal supplied from the outside; and

a pulse-number-control-data transfer setting step of setting pulse number control data that is set in advance corresponding to the interrupt factor distinguished at the interrupt factor

distinction step by transferring to a source supplying the operation clock by a program as microprocessor-clock-pulse-number control data.